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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/686,878	HSU ET AL.	
	Examiner	Art Unit	
	CARLTON V. JOHNSON	2436	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 October 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-8,10-22 and 24-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-8,10-22 and 24-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the Appeal Brief filed on 10/8/2009, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

/Nasser Moazzami/

Supervisory Patent Examiner, Art Unit 2436.

2. Claims **1, 3 - 8, 10 - 22, 24 - 30** are pending. Claims **2, 9, 23** have been cancelled. Claims **1, 10, 13, 17, 24, 28** are independent. This application was filed on 10-16-2003.

Response to Arguments

3. Applicant's arguments have been fully considered but are moot due to new grounds

of rejection.

3.1 The affidavits or declaration to overcome the Moiroux et al. reference for the rejection for claims 1, 3 - 8, 10 - 22, 24 - 30 are moot due to new grounds of rejection.

3.2 Ghosh discloses a TMA (Transportable Memory Apparatus) which is a self-contained and separate cache memory apparatus with battery backup capabilities. The TMA enables the contents of the cache memory, which consists of volatile memory, to be recoverable after a reboot procedure. The TMA in Ghosh prior art can detect a reduction in the power level of the computer system, which suggests an abnormal condition such as a power failure. Parameter(s) (PFAIL, BBEN flags) are set to perform activation or a reboot procedure. After the reboot procedure, the contents of the TMA can be saved to disk (non-volatile) storage. Due to battery backup, contents of cache memory are saved. (Ghost col. 6, lines 52-64; col. 9, line 52 - col. 10, line 9; col. 10, lines 17-23; col. 2, lines 13-15)

The completion of a reboot procedure can be performed and will accomplish the same result as the claimed invention, which is to quickly and definitely terminate all currently active processes without any processes stalling.

Ghosh prior art discloses software used to implement the functions of the prior art such as data save operations utilizing writes to hard disk drive with acknowledgements and system boot activation. Ghosh discloses the interaction of cache controller software with Operating System software such as kernel type software. The data save software disclosed within Ghosh is analogous to kernel type software and therefore

discloses kernel software. (Ghosh col. 1, lines 26-35; col. 10, lines 48-57)

3.3 Kamada discloses a kernel that specifically saves data (under the 103 rejection). (Kamada paragraph [0040], lines 7-9: kernel saves and manages class loader and thread group; kernel used to save data)

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims **1, 3 - 7, 10, 11, 13 - 21, 24 - 30** are rejected under 35 U.S.C. 102(e) as being anticipated by **Ghosh et al.** (US Patent No. **6,567,899**).

With Regards to Claim 1, Ghosh discloses an apparatus for rapidly, deterministically transferring data, the apparatus comprising:

a) a processor configured to process data; (Ghosh col. 3, lines 38-42: data transferred between a host processor and a memory storage device; col. 3, line 66 - col. 4, line 1: control bus for interconnecting memory apparatus with host processor)

b) a volatile memory configured to store the data; (Ghosh col. 3, lines 38-42: a memory storage device; col. 3, line 66 - col. 4, line 1: control bus for interconnecting memory apparatus with host processor; col. 2, lines 24-27: cache memory; when power fails or is interrupted, contents of cache is lost or corrupted (implies volatile memory if data lost when power is lost))

c) a boot control module configured to boot the processor with a standard operating kernel under a normal operating condition (Ghosh col. 6, lines 52-55: activation or power up sequence (boot procedure), provide cache memory, power source switching functions, and memory reconfiguration functions; col. 10, lines 48-57: module of code of software to perform functions (boot control module)) and to reboot the processor with a data transfer kernel (see Ghosh col. 6, lines 63-65: next activation or power up sequence (reboot); col. 10, lines 48-57: module of code of software to perform functions (data transfer module); col. 1, lines 26-35: cache controller interacts with operating system software to store data blocks on non-volatile storage) under an abnormal operating condition that threatens a loss of data in the volatile memory, wherein the reboot occurs without a loss of data within the volatile memory; (Ghosh col. 10, lines 17-23: computer system shutdown in battery backup mode for cache memory; col. 6, lines 52-64: power failure (abnormal operating condition); next activation or power up (reboot) sequence stored data (in cache memory and saved during reboot procedure) is downloaded to storage device)

Specification on page 5, lines 22-24 discloses that the reboot procedure is

specifically completed to quickly terminate all active processes and prevent process stalling. Ghosh discloses activation or reboot procedure which reset the processor and terminates all currently active processes.

d) the data transfer kernel configured to support a data save operation configured to save data in the volatile memory to a storage device. (Ghosh col. 6, lines 52-64: stored data downloaded to one or more disk drives during next activation or power up sequence (system boot or reboot); data transfer operation completed; col. 2, lines 24-27: cache memory; when power fails or is interrupted, contents of cache are lost or corrupted (implies volatile memory if data is lost when power is lost); col. 2, lines 13-15: power supply fails, data will be lost since cache memory is volatile; col. 1, lines 26-35; col. 10, lines 48-57: cache controller interfacing with OS for file transfer (acks))

With Regards to Claim 3, Ghosh discloses the apparatus of claim 1, wherein the data save operation is selected from the group consisting of a storage configuration operation, a transfer process loading operation, a data transfer operation, and a system shutdown operation. (Ghosh col. 6, lines 52-64: stored data downloaded to one or more disk drives during next activation or power up sequence (system boot or reboot); data transfer operation completed)

With Regards to Claims 4, 11, Ghosh discloses the apparatus of claims 3, 10, wherein the data transfer kernel is configured to support the data save operation. (Ghosh col. 6,

lines 52-64: stored data downloaded to a memory storage device; system on power up (reboot) supports save of data from cache memory to disk drives; col. 1, lines 26-35: cache controller interacts with operating system software to store data blocks on non-volatile storage)

With Regards to Claim 5, Ghosh discloses the apparatus of claim 1, further comprising a memory module comprising data bits for marking data to be saved during the data save operation. (Ghosh col. 12, lines 38-46: cache memory contains dirty data (data marked as modified and must be save to disk storage))

With Regards to Claim 6, Ghosh discloses the apparatus of claim 5, wherein the standard operating kernel is further configured to mark data to be saved during a data save operation. (Ghosh col. 12, lines 38-46: cache memory contains dirty data (data marked as modified and must be save to disk storage))

With Regards to Claims 7, 21, Ghosh discloses the apparatus, system of claims 1, 17, wherein the data transfer kernel is configured to configure a storage device for specialized data save operations. (Ghosh col. 10, lines 59-65: peripheral devices are configured; data control mechanism such as a SCSI controller is appropriately configured)

With Regards to Claims 8, 12, 22, Ghosh discloses the apparatus, system of claims 1,

10, 17, wherein the data transfer kernel is configured to conduct a power down sequence. (Ghosh col. 10, lines 17-23: system can be powered down; col. 6, lines 52-64: after next activation or power up sequence (reboot) cache memory data has been saved to a storage device; col. 1, lines 26-35; col. 10, lines 48-57: cache controller interfacing with OS for file transfer (acks))

With Regards to Claim 10, Ghosh discloses an apparatus for rapidly, deterministically transferring data to a storage device, the apparatus comprising:

a) a storage device configured to store data; (Ghosh col. 10, lines 59-65: peripheral devices are configured; data control mechanism such as a SCSI controller is appropriately configured)

b) a data transfer kernel configured to support data saving operations; (Ghosh col. 6, lines 52-64: stored data downloaded to a memory storage device; system on power up (reboot) supports save of data from cache memory to disk drives; col. 1, lines 26-35; col. 10, lines 48-57: cache controller interfacing with OS for file transfer (acks))

c) a computer in communication with the storage device, the computer configured to load the data transfer kernel during a reboot procedure (see Ghosh col. 6, lines 63-65: next activation or power up sequence (reboot); col. 10, lines 48-57: module of code of software to perform functions (data transfer module); col. 1, lines 26-35: cache controller interacts with operating system software to store data blocks on non-volatile storage) in response to an abnormal operating

condition that threatens the loss of data in a volatile memory, wherein the reboot procedure occurs without a loss of data in the volatile memory; (Ghosh col. 10, lines 17-23: computer system shutdown in battery backup mode for cache memory; col. 6, lines 52-64: power failure (abnormal operating condition); next activation or power up (reboot) sequence stored data (in cache memory and saved during reboot procedure) is downloaded to storage device)

Specification discloses that the reboot procedure is specifically completed to quickly terminate all active processes. Ghosh discloses an initialization which reset the processor and terminates all currently active processes.

d) the data transfer kernel configured to support a data save operation configured to save data in the volatile memory to the storage device. (Ghosh col. 6, lines 52-64: stored data downloaded to one or more disk drives during next activation or power up sequence (system boot or reboot); data transfer operation completed; col. 2, lines 24-27: cache memory; when power fails or is interrupted, contents of cache are lost or corrupted (implies volatile memory if data is lost when power is lost); col. 1, lines 26-35; col. 10, lines 48-57: cache controller interfacing with OS for file transfer (acks))

With Regards to Claim 13, Ghosh discloses an apparatus for rapidly, deterministically saving data, the apparatus comprising:

a) means for saving data in a non-volatile memory; (Ghosh col. 6, lines 52-64:

stored data downloaded to a storage device; col. 10, lines 48-57: module of code of software to perform functions (boot control module))

b) means for detecting a data save condition comprising an abnormal operating condition that threatens the loss of data in a volatile memory; (Ghosh col. 9, line 52 - col. 10, line 9: compare system power to a predetermined threshold; if system power falls below threshold voltage comparator will set PFAIL to 1)

With Regards to Claim 14, Ghosh discloses the apparatus of claim 13, further comprising means for configuring the means for saving data for data save operations. (Ghosh col. 10, lines 59-65: peripheral devices are configured; data control mechanism such as a SCSI controller, which controls associated disk drives, is appropriately configured)

With Regards to Claim 15, Ghosh discloses the apparatus of claim 13, further comprising means for booting a standard operating kernel for normal operation. (Ghosh col. 6, lines 52-55: activation or power up sequence (boot procedure), provide cache memory, power source switching functions, and memory reconfiguration functions)

With Regards to Claims 16, 27, 29, Ghosh discloses the apparatus, system, computer readable storage medium of claims 13, 24, 28, wherein comprising marking data to be saved during a data save operation. (Ghosh col. 12, lines 38-46: cache memory contains dirty data (data marked as modified and must be save to disk storage)) —

With Regards to Claim 17, Ghosh discloses a system for rapidly, deterministically saving data to a storage device, the system comprising:

a) a processor configured to process data; (Ghosh col. 3, lines 38-42: data transferred between a host processor and a memory storage device; col. 3, line 66 - col. 4, line 1: control bus for interconnecting memory apparatus with host processor)

b) a memory configured to provide volatile storage for the data; (Ghosh col. 3, lines 38-42: a memory storage device; col. 3, line 66 - col. 4, line 1: control bus for interconnecting memory apparatus with host processor; col. 2, lines 24-27: cache memory; when power fails or is interrupted, contents of cache is lost or corrupted (implies volatile memory if data lost when power is lost))

c) a storage device configured to provide non-volatile storage for the data; (Ghosh col. 10, lines 59-65: peripheral devices are configured; data control mechanism such as a SCSI controller is appropriately configured)

With Regards to Claim 18, Ghosh discloses the system of claim 17, wherein the standard operating kernel is configured to mark data in the memory to be saved by the data transfer kernel during a data save operation. (Ghosh col. 12, lines 38-46: cache memory contains dirty data (data marked as modified and must be save to disk storage))

With Regards to Claims 19, 30, Ghosh discloses the system, computer readable storage medium of claims 17, 28, wherein the data transfer kernel is configured to

support devices operations and processes required to save data. (Ghosh col. 6, lines 52-64: stored data downloaded to one or more disk drives during next activation or power up sequence (system boot or reboot); data transfer operation completed; col. 10, lines 48-57: module of code of software to perform functions (boot control module); col. 1, lines 26-35; col. 10, lines 48-57: cache controller interfacing with OS for file transfer (acks))

With Regards to Claim 20, Ghosh discloses the apparatus of claim 1, wherein the data transfer kernel is configured to support a data save operation. (Ghosh col. 6, lines 52-64: stored data downloaded to a memory storage device; system on power up (reboot) supports save of data from cache memory to disk drives; col. 1, lines 26-35; col. 10, lines 48-57: cache controller interfacing with OS for file transfer (acks))

With Regards to Claim 24, Ghosh discloses a method for rapidly, deterministically saving data, the method comprising:

a) detecting a data save condition comprising that threatens the loss of data in a volatile memory; (Ghosh col. 9, line 52 - col. 10, line 9: compare system power to a predetermined threshold; if system power falls below threshold voltage comparator will set PFAIL to 1)

b) rebooting a processor module with a data transfer kernel configured to support a data save operation configured to save the data in the volatile memory to a non-volatile storage device, wherein rebooting the processor module occurs without a

loss of data in the volatile memory. (Ghosh col. 6, lines 52-64: stored data downloaded to one or more disk drives during next activation or power up sequence (system boot or reboot); data transfer operation completed; col. 2, lines 24-27: cache memory; when power fails or is interrupted, contents of cache are lost or corrupted (implies volatile memory if data is lost when power is lost); stored data is saved; no loss of data in volatile memory; col. 1, lines 26-35; col. 10, lines 48-57: cache controller interfacing with OS for file transfer (acks))

With Regards to Claim 25, Ghosh discloses the method of claim 24, further comprising supporting devices, operations, and conducting processes required to save data to a storage device. (Ghosh col. 6, lines 52-64: stored data downloaded to one or more disk drives during next activation or power up sequence (system boot or reboot); data transfer operation completed; col. 10, lines 48-57: module of code of software to perform functions (boot control module)) –

With Regards to Claim 26, Ghosh discloses the method of claim 24, further comprising configuring the non-volatile storage device to receive data. (Ghosh col. 10, lines 59-65: peripheral devices are configured; data control mechanism such as a SCSI controller is appropriately configured)

With Regards to Claim 28, Ghosh discloses a computer readable storage medium comprising computer readable program code for rapidly, deterministically saving data,

the program code configured to:

a) boot a processor module in response to an abnormal operating condition that threatens the loss of data in a volatile memory module and in response to an abnormal operating condition that threatens the loss of data in a volatile memory module comprising volatile memory; (Ghosh col. 10, lines 17-23: computer system shutdown in battery backup mode for cache memory; col. 6, lines 52-64: power failure (abnormal operating condition); next activation or power up (reboot) sequence stored data (in cache memory and saved during reboot procedure) is downloaded to storage device)

b) transfer the data with the data save operation from the memory module to a non-volatile storage device. (Ghosh col. 6, lines 60-64: stored data downloaded to a storage device (non-volatile storage))

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims **1, 3 - 7, 10, 11, 13 - 21, 24 - 30** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ghosh et al.** (US Patent No. **6,567,899**) in view of **Kamada et**

al. (US PGPUB No. **20030149967**).

With Regards to Claim 1, Ghosh discloses an apparatus for rapidly, deterministically transferring data, the apparatus comprising:

a) a processor configured to process data; (Ghosh col. 3, lines 38-42: data transferred between a host processor and a memory storage device; col. 3, line 66 - col. 4, line 1: control bus for interconnecting memory apparatus with host processor)

b) a volatile memory configured to store the data; (Ghosh col. 3, lines 38-42: a memory storage device; col. 3, line 66 - col. 4, line 1: control bus for interconnecting memory apparatus with host processor; col. 2, lines 24-27: cache memory; when power fails or is interrupted, contents of cache is lost or corrupted (implies volatile memory if data lost when power is lost))

c) a boot control module configured to boot the processor with a standard operating kernel under a normal operating condition (Ghosh col. 6, lines 52-55: activation or power up sequence (boot procedure), provide cache memory, power source switching functions, and memory reconfiguration functions; col. 10, lines 48-57: module of code of software to perform functions (boot control module)) and to reboot the processor with a data transfer kernel (see Ghosh col. 6, lines 63-65: next activation or power up sequence (reboot); col. 10, lines 48-57: module of code of software to perform functions (data transfer module); col. 1, lines 26-35: cache controller interacts with operating system software to store data blocks on

non-volatile storage) under an abnormal operating condition that threatens a loss of data in the volatile memory, wherein the reboot occurs without a loss of data within the volatile memory; (Ghosh col. 10, lines 17-23: computer system shutdown in battery backup mode for cache memory; col. 6, lines 52-64: power failure (abnormal operating condition); next activation or power up (reboot) sequence stored data (in cache memory and saved during reboot procedure) is downloaded to storage device)

Specification on page 5, lines 22-24 discloses that the reboot procedure is specifically completed to quickly terminate all active processes and prevent process stalling. Ghosh discloses activation or reboot procedure which reset the processor and terminates all currently active processes.

d) the data transfer configured to support a data save operation configured to save data in the volatile memory to a storage device. (Ghosh col. 6, lines 52-64: stored data downloaded to one or more disk drives during next activation or power up sequence (system boot or reboot); data transfer operation completed; col. 2, lines 24-27: cache memory; when power fails or is interrupted, contents of cache are lost or corrupted (implies volatile memory if data is lost when power is lost); col. 2, lines 13-15: power supply fails, data will be lost since cache memory is volatile; col. 1, lines 26-35; col. 10, lines 48-57: cache controller interfacing with OS for file transfer (acks))

Ghosh discloses file transfer operations that interface with OS software. (see Ghosh

col. 1, lines 26-35; col. 10, lines 48-57: cache controller interfacing with OS for file transfer (acks))

Kernel software is OS type software and Ghosh discloses interfacing with OS software for data transfers.

Ghosh does not specifically disclose a kernel for saving data (data save kernel). However, Kamada discloses a data save kernel. (Kamada paragraph [0040], lines 7-9: kernel saves and manages class loader and thread group; kernel used to save data)

It would have been obvious to one of ordinary skill in the art to modify Ghosh for a kernel for saving data as taught by Kamada. One of ordinary skill in the art would have been motivated to employ the teachings of Kamada reduce memory and processing time when a plurality of application are executed. (see Kamada paragraph [0008], lines 1-6)

With Regards to Claim 3, Ghosh discloses the apparatus of claim 1, wherein the data save operation is selected from the group consisting of a storage configuration operation, a transfer process loading operation, a data transfer operation, and a system shutdown operation. (Ghosh col. 6, lines 52-64: stored data downloaded to one or more disk drives during next activation or power up sequence (system boot or reboot); data transfer operation completed)

With Regards to Claims 4, 11, Ghosh discloses the apparatus of claims 3, 10, wherein

the data transfer kernel is configured to support the data save operation. (Ghosh col. 6, lines 52-64: stored data downloaded to a memory storage device; system on power up (reboot) supports save of data from cache memory to disk drives; col. 1, lines 26-35: cache controller interacts with operating system software to store data blocks on non-volatile storage)

Ghosh discloses software for saving data as stated in Claim 1 above.

Kamada discloses kernel for saving data as stated in Claim 1 above.

With Regards to Claim 5, Ghosh discloses the apparatus of claim 1, further comprising a memory module comprising data bits for marking data to be saved during the data save operation. (Ghosh col. 12, lines 38-46: cache memory contains dirty data (data marked as modified and must be save to disk storage))

With Regards to Claim 6, Ghosh discloses the apparatus of claim 5, wherein the standard operating kernel is further configured to mark data to be saved during a data save operation. (Ghosh col. 12, lines 38-46: cache memory contains dirty data (data marked as modified and must be save to disk storage))

With Regards to Claims 7, 21, Ghosh discloses the apparatus, system of claims 1, 17, wherein the data transfer kernel is configured to configure a storage device for specialized data save operations. (Ghosh col. 10, lines 59-65: peripheral devices are configured; data control mechanism such as a SCSI controller is appropriately

configured)

With Regards to Claims 8, 12, 22, Ghosh discloses the apparatus, system of claims 1, 10, 17, wherein the data transfer kernel is configured to conduct a power down sequence. (Ghosh col. 10, lines 17-23: system can be powered down; col. 6, lines 52-64: after next activation or power up sequence (reboot) cache memory data has been saved to a storage device; col. 1, lines 26-35; col. 10, lines 48-57: cache controller interfacing with OS for file transfer (acks))

Ghosh discloses software for saving data as stated in Claim 1 above.

Kamada discloses a kernel for saving data as stated in Claim 1 above.

With Regards to Claim 10, Ghosh discloses an apparatus for rapidly, deterministically transferring data to a storage device, the apparatus comprising:

a) a storage device configured to store data; (Ghosh col. 10, lines 59-65: peripheral devices are configured; data control mechanism such as a SCSI controller is appropriately configured)

b) a data transfer kernel configured to support data saving operations; (Ghosh col. 6, lines 52-64: stored data downloaded to a memory storage device; system on power up (reboot) supports save of data from cache memory to disk drives; col. 1, lines 26-35; col. 10, lines 48-57: cache controller interfacing with OS for file transfer (acks))

c) a computer in communication with the storage device, the computer configured to

load the data transfer kernel during a reboot procedure (see Ghosh col. 6, lines 63-65: next activation or power up sequence (reboot); col. 10, lines 48-57: module of code of software to perform functions (data transfer module); col. 1, lines 26-35: cache controller interacts with operating system software to store data blocks on non-volatile storage) in response to an abnormal operating condition that threatens the loss of data in a volatile memory, wherein the reboot procedure occurs without a loss of data in the volatile memory; (Ghosh col. 10, lines 17-23: computer system shutdown in battery backup mode for cache memory; col. 6, lines 52-64: power failure (abnormal operating condition); next activation or power up (reboot) sequence stored data (in cache memory and saved during reboot procedure) is downloaded to storage device)

Specification discloses that the reboot procedure is specifically completed to quickly terminate all active processes. Ghosh discloses an initialization which reset the processor and terminates all currently active processes.

d) the data transfer kernel configured to support a data save operation configured to save data in the volatile memory to the storage device. (Ghosh col. 6, lines 52-64: stored data downloaded to one or more disk drives during next activation or power up sequence (system boot or reboot); data transfer operation completed; col. 2, lines 24-27: cache memory; when power fails or is interrupted, contents of cache are lost or corrupted (implies volatile memory if data is lost when power is lost); col. 1, lines 26-35; col. 10, lines 48-57: cache controller interfacing with OS

for file transfer (acks))

Ghosh discloses software for saving data as stated in Claim 1 above.

Kamada discloses kernel for saving data as stated in Claim 1 above.

With Regards to Claim 13, Ghosh discloses an apparatus for rapidly, deterministically saving data, the apparatus comprising:

a) means for saving data in a non-volatile memory; (Ghosh col. 6, lines 52-64: stored data downloaded to a storage device; col. 10, lines 48-57: module of code of software to perform functions (boot control module))

b) means for detecting a data save condition comprising an abnormal operating condition that threatens the loss of data in a volatile memory; (Ghosh col. 9, line 52 - col. 10, line 9: compare system power to a predetermined threshold; if system power falls below threshold voltage comparator will set PFAIL to 1)

Ghosh discloses software for saving data as stated in Claim 1 above.

Kamada discloses a kernel for saving data as stated in Claim 1 above.

With Regards to Claim 14, Ghosh discloses the apparatus of claim 13, further comprising means for configuring the means for saving data for data save operations. (Ghosh col. 10, lines 59-65: peripheral devices are configured; data control mechanism such as a SCSI controller, which controls associated disk drives, is appropriately configured)

With Regards to Claim 15, Ghosh discloses the apparatus of claim 13, further comprising means for booting a standard operating kernel for normal operation. (Ghosh col. 6, lines 52-55: activation or power up sequence (boot procedure), provide cache memory, power source switching functions, and memory reconfiguration functions)

With Regards to Claims 16, 27, 29, Ghosh discloses the apparatus, system, computer readable storage medium of claims 13, 24, 28, wherein comprising marking data to be saved during a data save operation. (Ghosh col. 12, lines 38-46: cache memory contains dirty data (data marked as modified and must be save to disk storage)) —

With Regards to Claim 17, Ghosh discloses a system for rapidly, deterministically saving data to a storage device, the system comprising:

a) a processor configured to process data; (Ghosh col. 3, lines 38-42: data transferred between a host processor and a memory storage device; col. 3, line 66 - col. 4, line 1: control bus for interconnecting memory apparatus with host processor)

b) a memory configured to provide volatile storage for the data; (Ghosh col. 3, lines 38-42: a memory storage device; col. 3, line 66 - col. 4, line 1: control bus for interconnecting memory apparatus with host processor; col. 2, lines 24-27: cache memory; when power fails or is interrupted, contents of cache is lost or corrupted (implies volatile memory if data lost when power is lost))

c) a storage device configured to provide non-volatile storage for the data; (Ghosh col. 10, lines 59-65: peripheral devices are configured; data control mechanism

such as a SCSI controller is appropriately configured)

Ghosh discloses software for saving data as stated in Claim 1 above.

Kamada discloses a kernel for saving data as stated in Claim 1 above.

With Regards to Claim 18, Ghosh discloses the system of claim 17, wherein the standard operating kernel is configured to mark data in the memory to be saved by the data transfer kernel during a data save operation. (Ghosh col. 12, lines 38-46: cache memory contains dirty data (data marked as modified and must be save to disk storage))

With Regards to Claims 19, 30, Ghosh discloses the system, computer readable storage medium of claims 17, 28, wherein the data transfer kernel is configured to support devices operations and processes required to save data. (Ghosh col. 6, lines 52-64: stored data downloaded to one or more disk drives during next activation or power up sequence (system boot or reboot); data transfer operation completed; col. 10, lines 48-57: module of code of software to perform functions (boot control module); col. 1, lines 26-35; col. 10, lines 48-57: cache controller interfacing with OS for file transfer (acks))

Ghosh discloses software for saving data as stated in Claim 1 above.

Kamada discloses a kernel for saving data as stated in Claim 1 above.

With Regards to Claim 20, Ghosh discloses the apparatus of claim 1, wherein the data transfer kernel is configured to support a data save operation. (Ghosh col. 6, lines 52-

64: stored data downloaded to a memory storage device; system on power up (reboot) supports save of data from cache memory to disk drives; col. 1, lines 26-35; col. 10, lines 48-57: cache controller interfacing with OS for file transfer (acks))

Ghosh discloses software for saving data as stated in Claim 1 above.

Kamada discloses a kernel for saving data as stated in Claim 1 above.

With Regards to Claim 24, Ghosh discloses a method for rapidly, deterministically saving data, the method comprising:

a) detecting a data save condition comprising that threatens the loss of data in a volatile memory; (Ghosh col. 9, line 52 - col. 10, line 9: compare system power to a predetermined threshold; if system power falls below threshold voltage comparator will set PFAIL to 1)

b) rebooting a processor module with a data transfer kernel configured to support a data save operation configured to save the data in the volatile memory to a non-volatile storage device, wherein rebooting the processor module occurs without a loss of data in the volatile memory. (Ghosh col. 6, lines 52-64: stored data downloaded to one or more disk drives during next activation or power up sequence (system boot or reboot); data transfer operation completed; col. 2, lines 24-27: cache memory; when power fails or is interrupted, contents of cache are lost or corrupted (implies volatile memory if data is lost when power is lost); stored data is saved; no loss of data in volatile memory; col. 1, lines 26-35; col. 10, lines 48-57: cache controller interfacing with OS for file transfer (acks))

Ghosh discloses software for saving data as stated in Claim 1 above.

Kamada discloses a kernel for saving data as stated in Claim 1 above.

With Regards to Claim 25, Ghosh discloses the method of claim 24, further comprising supporting devices, operations, and conducting processes required to save data to a storage device. (Ghosh col. 6, lines 52-64: stored data downloaded to one or more disk drives during next activation or power up sequence (system boot or reboot); data transfer operation completed; col. 10, lines 48-57: module of code of software to perform functions (boot control module))

Ghosh discloses software for saving data as stated in Claim 1 above.

Kamada discloses a kernel for saving data as stated in Claim 1 above.

With Regards to Claim 26, Ghosh discloses the method of claim 24, further comprising configuring the non-volatile storage device to receive data. (Ghosh col. 10, lines 59-65: peripheral devices are configured; data control mechanism such as a SCSI controller is appropriately configured)

With Regards to Claim 28, Ghosh discloses a computer readable storage medium comprising computer readable program code for rapidly, deterministically saving data, the program code configured to:

a) boot a processor module in response to an abnormal operating condition that threatens the loss of data in a volatile memory module and in response to an

abnormal operating condition that threatens the loss of data in a volatile memory module comprising volatile memory; (Ghosh col. 10, lines 17-23: computer system shutdown in battery backup mode for cache memory; col. 6, lines 52-64: power failure (abnormal operating condition); next activation or power up (reboot) sequence stored data (in cache memory and saved during reboot procedure) is downloaded to storage device)

b) transfer the data with the data save operation from the memory module to a non-volatile storage device. (Ghosh col. 6, lines 60-64: stored data downloaded to a storage device (non-volatile storage))

Ghosh discloses software for saving data as stated in Claim 1 above.

Kamada discloses a kernel for saving data as stated in Claim 1 above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Carlton V. Johnson whose telephone number is 571-270-1032. The examiner can normally be reached on Monday thru Friday , 8:00 - 5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nasser Moazzami can be reached on 571-272-4195. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

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/Nasser Moazzami/
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CVJ
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